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No. of Printed Pages—4 **CS–702**

B. TECH.

SEVENTH SEMESTER EXAMINATION, 2003-2004

COMPUTER ARCHITECTURE

Time : 3 Hours *Total Marks : 100*

Note : Attempt **ALL** the questions.

1. Answer any TWO of the following :— **(10×2=20)**

(a) Discuss the Flynn's classification of various computer architectures with the help of their functional block diagram.

(b) Explain how Instruction set, Memory hierarchy, Compiler technology, CPU implementation and Control affect the CPU performance and justify the effect in terms of program length, clock rate and effective CPI.

(c) Define CPI (Cycle Per Instruction) and MIPS (Million Instructions Per Second) rate. Determine the effective CPI, MIPS rate and execution time for the following program executed by 40 MHz processor :—

Clock Cycle Count and Instruction Mix of the Program :

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmetic	45000	1
Data Transfer	32000	2
Floating Point	15000	2
Control Transfer	800	2

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2. Answer any TWO of the following :— (10×2=20)

(a) Discuss the CISC and RISC architectures with the help of their functional block diagrams. Also indicate their advantages and drawbacks.

(b) Explain how the Degree Of Parallelism (DOP) and number of processors affect the performance of a parallel computing system. Give Amdahl's law and find the expression for fixed load speedup.

(c) Describe the set-associative organization of cache memory. Consider a cache (M_1) and main memory (M_2) hierarchy with the following characteristics :—

M_1: 16 K words, 50 ns access time

M_2: 1 M words, 400 ns access time

Assume 8 word cache blocks and a set size of 256 words with set associative mapping.

(i) Show the mapping between M_1 and M_2

(ii) Calculate the effective memory access time with the cache bit ratio of h = 0.95.

3. Answer any TWO of the following :— (10×2=20)

(a) Design a binary integer multiply pipeline with five stages. The first stage is for partial product generation. The last stage is a 36-bit Carry-Lookahead Adder (CLA). The middle three stages are made of 16 carry-save adders (CSA) of appropriate lengths.

(i) Prepare a schematic design of the five-stage multiply pipeline. All line widths and interstage connections must be shown.

(ii) Determine the maximal clock rate of the pipeline if the stage delays are $\tau_1 = \tau_2 = \tau_3 = \tau_4 = 90$ ns, $\tau_5 = 45$ ns and the latch delay is 20 ns.

(b) Discuss the various possible hazards between read and write operations in an instruction pipeline and state the mechanism to detect and avoid these hazards. Also discuss the Tomasulo's algorithm for dynamic instruction scheduling.

(c) Explain the structure of Superscalar Pipeline. Give functional block diagram of 2-issue superscalar processor and discuss the execution of a sample program.

4. Answer any TWO of the following :— **(10×2=20)**

(a) Discuss the principles of vector processing. Also explain various types of vector instructions and their execution.

(b) Explain the following loop transformations and discuss how to apply them for loop vectorization or parallelization :—

(i) Loop Permutation
(ii) Loop Reversal
(iii) Loop Skewing
(iv) Loop Tiling

(c) Consider the following loopnest :—

```
Do    I = 1, N
      Do J = 2, N
S1:   A(I, J) = B (I, J) + C(I, J)
S2:   C(I, J) = D (I, J) / 2
S3:   E(I, J) = A (I, J-1) **2+E(I, J-1)
      Enddo
Enddo
```

(i) Show the data dependence among the statements.

(ii) Show how to parallelize the loop scheduling the parallelizable iterations to concurrent processors.

5. Answer any TWO of the following :— **(10×2=20)**

(a) Explain how following factors affect the performance of an inter-connection network :—

(i) Functionality

(ii) Network Latency

(iii) Bandwidth

(iv) Hardware Complexity

(b) Answer the following questions related to multistage networks :—

(i) How many legitimate states are there in a 4×4 switch module, including both broadcast and permutations ? Justify your answer with reasoning.

(ii) Construct a 64-input omega network using 4×4 switch modules in multiple stages. How many permutations can be implemented directly in a single pass through the network without blocking ?

(c) Write short notes on the following :—

(i) Hypercube Routing Function

(ii) Crossbar Switches

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